CDA 4203L Sec 001

Computer System Design Lab

Lab 5 Report

GCD FSM and Datapath

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| --- | --- |
| Today’s Date: |  |
| Team Members: |  |
|  |
|  |
| Work Distribution: | Briefly explain the tasks completed by each team member |
| No. of Hours Spent: |  |
| Exercise Difficulty:  (Easy, Average, Hard) |  |
| Any Other Feedback: |  |

**Problem 1:** Show the state diagram of your GCD controller and behavioral components in the data path. Briefly explain how the design works. *Use as many pages as needed.*

**Problem 1:** Include the structural Verilog code of (a) data path components; behavioral Verilog code of (b) FSM; (c) Testbench; and (d) Simulation waveforms. *Use as many pages as needed.*

**Problem 2:** Include (a) the **.ucf** file; and (b) synthesis report. *Use as many pages as needed.*